REMARKS

Summary of Claim Status

Claims 1-19 are pending in the present application. Claims 1-19 are rejected for the reasons discussed below. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections in view of the present amendment and in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1-5 and 7-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jain, U.S. Patent No. 6,038,386 ("Jain"). Applicants respectfully disagree and traverse the rejection with regard to all claims, submitting that Jain does not teach or even suggest the claimed invention. Furthermore, Applicants have amended Claim 1 in the interest of advancing prosecution to point out more particularly and claim distinctly the subject matter which Applicants regard as the invention, thus rendering the rejection moot.

Claim 1 recites assigning a first supply voltage to operate a first set of one or more active blocks of the programmable logic device, and assigning a second supply voltage, less than the first supply voltage, to operate a second set of one or more active blocks of the programmable logic device. Applicants respectfully submit that Jain does not teach at least such features.

The Office Action alleges that Col. 3, lines 61-67, Fig. 5, and Col. 8, lines 63-66 teaches assigning a first supply voltage to operate a first set of one or more active blocks. However, those cited portions appear to teach only that some PLDs (programmable logic devices) provide users the capability of controlling power consumption by operating macrocells in a high power or low power mode, with no mention of first or second supply voltages. In fact, Jain teaches that high and lower power modes are controlled in two ways, neither relying on multiple voltages. In Jain, at the AND-term level, power consumption is controlled by controlling a leaker path for a sense amplifier. See Jain at Col. 5, lines 65-67. Jain further teaches that power

consumption at the OR-term level is controlled by a bit that turns on one of two transistors of different sizes. See Jain at Col. 6, lines 17-28.

Thus, in Jain, power levels may be controlled either by activating a leaker path in a sense amplifier or by changing transistor sizing, and not by assigning a first and second supply voltage as recited in Claim 1.

Moreover, Applicants have amended Claim 1 to recite determining a plurality of timing slacks for each of a plurality of active blocks of the design, and determining a minimum timing slack for each of the plurality of active blocks of the design. Thus, each active block may have a plurality of timing slacks, and a minimum timing slack is determined and used to assign the first and second supply voltages.

In contrast, Jain does not teach or even suggest determining a plurality of timing slacks for each of a plurality of active blocks, and then determining a minimum timing slack for each active block. Instead, Jain teaches optimizing power along a single timespec path by taking the slack in the timespec path and the additional delay incurred for switching a Macrocell to low power, and determining the maximum number of Macrocells that can be switched to low power. See Jain at Col. 12, line 63 to Col. 13, line 42. Jain does not even mention, much less teach or suggest, a minimum timing slack as recited in Claim 1.

Therefore, Applicants believe Claim 1 is allowable over Jain, and respectfully request allowance of Claim 1.

Claims 2-5 and 7-11 depend, either directly or indirectly, from Claim 1, and thus include all of the limitations of Claim 1. Applicants believe Claim 1 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claims 2-5 and 7-11 are also allowable, and respectfully requests allowance of such claims.

All of the above amendments are fully supported by the specification, for example in Figure 7 and the corresponding text.

Rejections Under 35 U.S.C. § 103

Claims 6 and 12-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of Mizuno et al., U.S. Patent Publication No.

2004/0145955 ("Mizuno"). Applicants respectfully disagree and traverse the rejection with regard to all claims, submitting that Jain and Mizuno, alone or in any combination, do not teach the claimed inventions. In particular, Applicants submit that *prima facie* obviousness has not been established. Furthermore, Applicants believe the present amendments render the rejections moot.

The Office Action admits that Jain does not disclose the use of a third voltage. Mizuno is cited by the Office Action as "disclos[ing] a method for controlling power consumption in a semiconductor integrated circuit that include the use of a third voltage." See Office Action at page 5. The Office Action further states that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the use of a third voltage course in the method of Mizuno in the method of Jain because this would improve Jain's invention since a third voltage source aids in optimization of a circuit block," citing Jain at Col. 11, lines 55-59.

However, the cited portion of Jain merely states that a power mode associated with each Macrocell and a slew rate associated with each I/O module, which can either be a default setting or specified by the user. There is no apparent teaching or suggestion regarding any voltage source, and there is no mention of any deficiency or shortcoming of the method in Jain that would require combination with Mizuno. Specifically, there is nothing in Jain to suggest that any aid in optimization of a circuit block is necessary, or that "a third voltage source aids in optimization of a circuit block."

Further, Mizuno does not teach the use of a third voltage in a method for controlling power consumption. Mizuno, in fact, relates to a circuit for operating internally stably in spite of the use of a fluctuating voltage. See, e.g., Mizuno at Abstract. That is, Mizuno addresses the problem of large power-supply noise (see, e.g., Mizuno at [0012], lines 7-10) caused by large current flows to one circuit affecting the very-low voltage supplied to DRAM, ADC, DAC, PLL, flash memory, microprocessor, or DSP circuits that are sensitive to fluctuations in the power supply (see, e.g., Mizuno at [0012], lines 21-30). Thus, Mizuno is concerned with minimizing power supply fluctuation or noise, and does not appear to teach or suggest methods for reducing power consumption.

Therefore, Applicants believe it would not have been obvious for one of skill in the art to combine Jain and Mizuno in the manner proposed by the Office Action, since there is nothing in Jain to suggest that the method would be improved by the combination, and Mizuno deals with an entirely different problem. Applicants therefore believe Claims 6 and 12-14 are allowable, and allowance of such claims is respectfully requested.

With respect to Claim 6, which depends from Claim 1, Applicants believe the present amendment in Claim 1 overcomes all rejections. That is, as noted above, Jain fails to teach or suggest the additional features recited in Claim 1, and Mizuno does not remedy the failings of Jain. For this additional reason, Claim 6 is further believed to be allowable.

With respect to Claim 12, Applicants have further amended Claim 12 to recite that the operating voltage is selected in response to the minimum timing slack, determined from a plurality of timing slacks, associated with the programmable logic block. As noted above, Jain does not teach or disclose such a minimum timing slack, and Mizuno does not remedy this failing in Jain. Therefore, for at least this additional reason, Claim 12 is further believed to be allowable.

Claims 13 and 14 depend from Claim 12, and thus include all of the limitations of Claim 12. Applicants believe Claim 12 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claims 13 and 14 are also allowable, and respectfully requests allowance of such claims.

Claims 15-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of Mizuno and further in view of Almulla, U.S. Patent No. 5,612,892 ("Almulla"). Applicants respectfully disagree and traverse the rejection with regard to all claims, submitting that Jain, Mizuno, and Almulla, alone or in any combination, do not teach the claimed inventions. In particular, Applicants submit that *prima facie* obviousness has not been established. Furthermore, Applicants believe the present amendments render the rejection moot.

Claim 15 depends from Claim 12, and thus includes all of the limitations of Claim 12. Applicants believe Claim 12 is allowable for the reasons set forth above.

Therefore, for at least the same reasons, Applicants believe Claim 15 is also allowable, and respectfully requests allowance of Claim 15.

Applicants have amended Claim 16 to recite a means for controlling the first and second voltage switches such that each of the programmable logic blocks having an associated minimum timing slack less than a threshold timing slack is coupled to receive the first supply voltage, and each of the programmable logic blocks having an associated minimum timing slack greater than the threshold timing slack is coupled to receive the second supply voltage.

First, Applicants submit that Jain does not even mention, much less teach or suggest, any threshold timing slack as recited in Claim 16. None of the secondary references Mizuno or Almulla appear to mention any such threshold timing slack. If the rejection is to be maintained, Applicants respectfully request clarification as to the specific teaching in the references that discloses such a feature.

Moreover, as noted in greater detail above, Jain does not teach or suggest a minimum timing slack, and Mizuno and Almulla do not remedy the failings in Jain. Therefore, Applicants believe Claim 16 is allowable for this further reason.

Claims 17-19 depend from Claim 16, and thus include all of the limitations of Claim 16. Applicants believe Claim 16 is allowable for the reasons set forth above. Therefore, for at least the same reasons, Applicants believe Claims 17-19 are also allowable, and respectfully requests allowance of Claims 17-19.

Conclusion

Applicant acknowledges an unusually thorough and helpful analysis of all pending claims by the Examiner.

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believe that Claims 1-19 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on June 22, 2006.

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Signature